High Level Synthesis with a Dataflow Architectural Template

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ABSTRACT

In this work, we present a new approach to high level synthesis (HLS), where high level functions are first mapped to an architectural template, before hardware synthesis is performed. As FPGA platforms are especially suitable for implementing streaming processing pipelines, we perform transformations on conventional high level programs where they are turned into multi-stage dataflow engines. This target template naturally overlaps slow memory data accesses with computations and therefore has much better tolerance towards memory subsystem latency. Using a state-of-the-art HLS tool for the actual circuit generation, we observe up to 9x improvement in overall performance when the dataflow architectural template is used as an intermediate compilation target.

Keywords

FPGA, Overlay Architecture, Hardware design template, High-level Synthesis, Pipeline Parallelism

1. INTRODUCTION

As the complexity of both the FPGA devices and their applications increase, the task of efficiently mapping the desired functionality is getting ever more challenging. To alleviate the difficulty of designing for FPGAs, there has been a trend towards using higher levels of abstraction. Tools taking in high-level function specifications and generating hardware IP blocks have been developed both in academia [1, 2] and industry [3, 4]. Of course, the semantics of the high level languages like C/C++ are vastly different than the description of hardware behavior at clock cycle granularity. The tools often try to bridge this gap by fitting the control data flow graph (CDFG) of the original program into particular hardware paradigms such as Finite State Machine with Datapath (FSMD). Depending on the nature of the application, these approaches may or may not generate hardware taking full advantage of what the FPGA has to offer. User guidance in the forms of directives or pragmas are often needed to expose parallelism of various kinds and to optimize the design. An important dimension of the space is in the mechanism with which memory data are accessed. Designers sometimes need to restructure the original code to separate out memory accesses before invoking HLS. Also, it is often desirable to convert from conventional memory accesses to a streaming model and to insert DMA engines [5]. Further enhancements can be achieved by including accelerator specific caching and burst accesses.

In this paper, we realize an intermediate architectural template (section 2) that will complement existing work in HLS. It captures some of the common patterns applied in optimizing HLS generated designs. In particular, by taking advantage of the FPGAs as throughput-oriented devices, it structures the computation and data accesses into a series of coarse-grained pipeline stages, through which data flows. To target this architectural template, we have developed a tool to slice the original CDFG of the performance critical loop nests into subgraphs, connected by communication channels (section 3). This decouples the scheduling of operations between different subgraphs and subsequently improves the overall throughput in the presence of data fetch stalls. Then, each of the subgraphs is fed to a conventional high-level synthesis flow, generating independent datapaths and controllers. FIFO channels are instantiated to connect the datapaths, forming the final system (section 4). The performance, when compared against directly synthesized accelerators, is far superior (section 5), demonstrating the advantage of targeting the dataflow architectural template during HLS.

2. THE DATAFLOW ARCHITECTURAL TEMPLATE

Currently, HLS tools use a simple static model for scheduling operations. Different parts of the generated hardware run in lockstep with each other, with no need for dynamic dependency checking mechanisms such as scoreboard or load-store queuing. This rigid scheduling of operators, while producing circuit of simpler structure and smaller area, is vulnerable to stalls introduced by cache misses or variable latency operations. The entire compute engine is halted as the state machine in the controller waits for the completion of an outstanding operation. This effect becomes very pronounced when irregular offchip data accesses are encoded in the function. Under these circumstances, the traditional approach where data movements are explicitly managed using DMA may not be effective as the access pattern is not known...
statically. Also, there may not be sufficient on-chip memory to buffer the entirety of the involved data structure. As a result, the overall performance can deteriorate significantly.

To alleviate this problem, instead of directly synthesizing the accelerator from the original control dataflow graph, we first map the input function to an architecture resembling a dataflow engine. Figure 1 illustrates this mapping for a very simple example. The original function is broken up into a set of communicating processes, each of which can be individually turned into an accelerator. The memory subsystem is assumed to be able to take in multiple outstanding requests.

The mapping process can distribute operations in the original function into multiple stages. This process can of course generate a large number of potential implementations. At one end of the spectrum, the entire function is fit into a single stage—in which case we have a typical HLS generated accelerator, where everything is coupled with everything else through the static schedule. At the other end of the spectrum, each individual operation can be scheduled independently as a standalone module, getting activated whenever its inputs are available—we essentially have a fine grained dataflow machine with very high area overhead. The optimal design points lie somewhere in between these two extremes. In section 3, we present one partitioning algorithm which aims to localize data fetch stalls, and thus addresses the main factor for the performance degradation mentioned earlier. It by no means covers the entire space of different partitioning granularity, but should have reaped most of the benefits in mapping to this intermediate dataflow architecture.

For our example, the change in overall execution schedule can be seen in figure 2. The occasional off-chip data fetches no longer affect the performance of the processing engine as the long latency floating point multiply shadows the stalls introduced by these cache misses. As long as the overall bandwidth provided by the memory subsystem can satisfy the computation, the latency of memory accesses can be tolerated. This overlapping of computation and communication is naturally provided by the architecture, and provides significant boost in performance, as will be shown later.

3. MAPPING TO THE DATAFLOW ARCHITECTURAL TEMPLATE

Mapping from a standard CDFG to the dataflow architectural template involves a partitioning process where dependency edges are cut and nodes are assigned to different stages in the pipeline template. To maximize the performance of the final circuit, several factors need to be considered during this partitioning process. First, circular dependencies between nodes need to be contained within stages. These strongly connected components (SCCs) in CDFG are associated with loop carried dependencies, and are the limiting factors for how aggressively loop iterations can be overlapped. The initiation interval (II) of loops are dictated by the latency of these cycles. As the communication channels will always add latency, having parts of a SCC distributed across different stages would increase the II of the iterations, as they are now executed in a distributed manner. The same observation was made in [6], albeit in a different context.

Secondly, as we have shown in section 2, with memory operations separated from dependency cycles involving long latency computation, we can have cache misses completely hidden by the slow rate of data consumption. Thirdly, to localize the effects of stalls introduced by cache misses, the number of memory operations in each stage should be minimized, especially when they address different parts of the memory space.

3.1 The Partitioning Algorithm

In Algorithm 1, the steps taken to achieve the aforementioned requirements are detailed. The SCCs are collapsed into new nodes, which together with the original nodes in the CDFG, are topologically sorted. The obtained directed acyclic graph is traversed and a new pipeline stage in the template is created whenever a memory operation or an SCC with long latency computation is encountered. Here, long latency operations are those which cannot be completed within one clock cycle. The details of the hardware device and the design’s timing constraints determine which operations are long latency. In our experiments, we leverage Xilinx’s Vivado HLS to generate the these timing numbers. With a target clock frequency of 150MHz, for instance, a 32 bit integer addition can be completed within a one clock cycle while a floating point multiply takes four cycles. These numbers are accurate as we eventually use Vivado HLS for our HDL generation.

The semantics of the input high level language often cre-
Figure 2: Execution schedule of accelerator with and without mapping to dataflow architecture

Algorithm 1 Partitioning algorithm

1: procedure PARTITIONCDFG(G)  
2:  SCCs ← allStronglyConnComps(G)  
3:  DAG ← collapse(SCCs, G)  
4:  TopoSortedNodes ← topologicalSort(DAG)  
5:  LongSCCs ← getSCCWithLongOp(SCCs)  
6:  MemNodes ← findLdStNodes(G)  
7:  MemLongSCC ← LongSCCs ∪ MemNodes  
8:  allStages ← {}  
9:  curStage ← {}  
10: while TopoSortedNodes ≠ ∅ do  
11:  curNode ← TopoSortedNodes.pop()  
12:  curStage ← curStage ∪ curNode  
13:  if curNode ∈ MemLongSCC then  
14:    allStages ← allStages ∪ curStage  
15:    curStage ← {}  
16:  end if  
17:  end while  
18: return allStages  
19: end procedure

As the decoupled processing modules are eventually connected together to form a pipeline, each pair of communication primitives inserted requires an instantiation of a FIFO. On FPGAs, the area costs for FIFOs, even ones with a relatively small number of entries, can be significant. Consequently it is often better to duplicate some computation rather than creating a new hardware queue between two modules. Currently, we do not duplicate long latency computation (e.g., multiply) or memory accesses as these are the operations we aimed to separate during the partitioning step. However, some of the most frequently occurring SCCs, i.e., increment of loop counters, still provide opportunities for this optimization.

3.2 Potential Optimizations

3.2.1 Trade-off Between Computation and Communication

As the decoupled processing modules are eventually connected together to form a pipeline, each pair of communication primitives inserted requires an instantiation of a FIFO. On FPGAs, the area costs for FIFOs, even ones with a relatively small number of entries, can be significant. Consequently it is often better to duplicate some computation rather than creating a new hardware queue between two modules. Currently, we do not duplicate long latency computation (e.g., multiply) or memory accesses as these are the operations we aimed to separate during the partitioning step. However, some of the most frequently occurring SCCs, i.e., increment of loop counters, still provide opportunities for this optimization.

3.2.2 Memory Optimization

As mentioned in section 3.1, after a memory operation is added to a stage, a new stage is created. All the consumers of the data requested are thus decoupled from the stage issuing the memory request. This transformation allows for many outstanding requests to be pipelined into the memory subsystem. For accessing consecutive memory locations, these operations are automatically converted to burst
accesses, improving efficiency of memory bandwidth usage.

In our flow, the partitioning of the memory space has also provided an opportunity to better customize the hardware for memory access on the FPGA fabric. Each independent data access interface, corresponding to one memory partition, can be supported differently according to the nature of the address stream it generates. For instance, when streaming type loads are concatenated into bursted accesses, they would not benefit from having on-chip buffer due to the absence of data reuse, while random memory accesses can be helped with a general purpose cache, whose size and associativity can be tuned according to the runtime profile.

4. HARDWARE GENERATION

With the high level function mapped to the dataflow architecture, we then leverage conventional HLS tools for the RTL generation. The mapping step described in section 3 is based on the LLVM infrastructure [7]. The LLVM front end parses C/C++ functions and convert them into the single static assignment (SSA) form, that facilitates dependency tracking between operations, making the implementation of the algorithm easier. To provide HLS tools with a valid input, we convert the LLVM intermediate representation for each stage in the pipeline to synthesizable C, with a complementary TCL script to drive the tool and connect the stages with FIFOs.

The approach we take in converting LLVM IR to C is rather simplistic. Instead of recovering the higher level semantics, we simply generate a one to one mapping of each LLVM instruction to C statement. The only common llvm instruction which does not have a simple equivalence in C is the operation, which assigns values based on the predecessor of the current basic block. Our flow creates a different operation itself is then removed.

The steps involved, i.e., mapping of the original input function to the architecture template and the partitioning and hardware generation, are summarized in figure 3.

5. EXPERIMENTAL EVALUATION

To evaluate the benefits of our approach, we took several benchmark kernels and processed them with our flow. For sparse matrix vector (SpMV) multiply—our first kernel—compressed sparse row (CSR) format is used to store the matrix, where the loads of the floating point numbers to be multiplied depend on the data in an index array. The next two kernels, Knapsack and Floyd-Warshall, are both dynamic programming problems. The memory addresses to be accessed are derived from the results of computation. Our final kernel, Depth first search (DFS), is a widely used graph algorithm. The benchmark version operates on pointer based data structure and uses a stack. All these kernels are sequential code with non-regular control flow and memory access patterns. The input dataset for each benchmark, as described by Table 1, is also too big to fit entirely on chip. Due to the presence of statically unknown off-chip memory accesses, these benchmarks are good cases where our algorithm can play a significant role in improving the overall performance. On the other hand, for problems where the entire data set can be buffered on chip or when the memory access patterns are regular, our approach would offer little performance advantage over the conventional DMA+accelerator approach [5].

Table 1: Input Data Set for the Benchmarks

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Description of Input Data</th>
<th>Size of Input Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>SpMV Multiply</td>
<td>Matrix dimension = 4096</td>
<td>≈ 16 MB</td>
</tr>
<tr>
<td></td>
<td>Density of Matrix = 0.25</td>
<td></td>
</tr>
<tr>
<td>Knapsack</td>
<td>Weight Limit = 3200</td>
<td>≈ 5 MB</td>
</tr>
<tr>
<td></td>
<td>Number of Items = 200</td>
<td></td>
</tr>
<tr>
<td>Floyd-Warshall</td>
<td>Number of Nodes = 1024</td>
<td>≈ 8 MB</td>
</tr>
<tr>
<td>Depth-First Search</td>
<td>Number of Nodes = 4000</td>
<td>≈ 3 MB</td>
</tr>
<tr>
<td></td>
<td>Number of Neighbors per Node = 200</td>
<td></td>
</tr>
</tbody>
</table>

The FPGA device used for our evaluation is the Zynq-7000 XC7Z020 FPGA SoC from Xilinx, installed on the Zed-Board evaluation platform. The SoC contains two parts: an ARM-processor based processing system (PS), and the programmable logic (PL). The baseline for our evaluation is the performance of each software kernel running on the ARM core in the PS. The core is an out-of-order, dual-issue hard processor running at 667MHz. The Zynq platform also provides two options for the accelerators in PL to access the main memory subsystem: through the accelerator coherence port (ACP), or the high performance (HP) port. The former connects to the snoop control unit in the processing system and thus uses/modifies the processing system’s on chip cache. The HP port connects directly to the memory controller, which necessitates the flushing of cache lines by the processor if cached memory is accessed by the accelerator. In either case, if memory states are also buffered in the PL with caches, they need to be explicitly pushed to the processing system side after the accelerator finishes running. As both the ACP and the HP are slave ports, they provide no mechanisms to extract data from the programmable logic when the ARM processor is running. The interaction between the generated accelerators and the main pieces of the FPGA SoC is shown in figure 4.
5.1 Performance Comparisons

In figure 5, performance of the different implementations are presented. Conventional accelerators and dataflow accelerators with different memory subsystem configurations are compared. All the numbers are normalized to the baseline.

In all four benchmarks, conventional accelerators directly generated from software kernels using the HLS flow actually have lower performance than the hard processor. Even with on-PL caches, these accelerators only manage to achieve throughput less than 50% that of the baseline. The superscalar, out-of-order ARM core is capable of exploiting instruction level parallelism to a good extent and also has a high performance on-chip cache. The additional parallelism extracted by the HLS tool is evidently not enough to compensate for the clock frequency advantage the hard processor core has over the programmable logic and the longer data access latency from the reconfigurable array.

With our methodology, the processing pipelines generated are rather competitive against the hard processor, even without a reconfigurable cache. For SpMV multiply, knapsack and Floyd-Warshall, when the dataflow accelerators are directly connected to the PS through the ACP, the average performance is 2.3x that of the baseline— representing an 8.4x gain over the conventional accelerators. Upon the addition of caches, the average runtime of the dataflow accelerators was reduced by 18.7%, while that of the conventional accelerators was cut by 45.4%. The gap between their performance is thereby reduced from 8.4 to 5.6 times. This difference in improvement is due to conventional accelerators' sensitivity to the latency of data accesses, which is also manifested by its performance degradation of 40% when the uncached HP port is used instead of ACP.

It is also apparent that our approach has its limitations, as demonstrated by its ineffectiveness in the depth first search benchmark. The kernel performs very little computing but lots of memory accesses. The use of a stack in DFS also manifests by its performance degradation of 40% when the uncached HP port is used instead of ACP.

5.2 Area comparison

Overall, for kernels suitable for FPGA acceleration, there is a significant performance advantage in using an intermediate dataflow architectural template. If we compare the best results achieved with the dataflow accelerators to that of the conventional accelerators, we see improvement of 3.3 to 9.1 times, with an average of 5.6.
To quantify the impact of our proposed methodology on area, we have compared the FPGA resource usage of conventional accelerators and the dataflow accelerators. Table 2 shows the results, where each accelerator is complemented with two different memory subsystem configurations.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>ACP</th>
<th>ACP + 64KB Cache</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LUT</td>
<td>FFs</td>
</tr>
<tr>
<td>SpMV Multiply</td>
<td>Con. Acc</td>
<td>9873</td>
</tr>
<tr>
<td></td>
<td>Dataflow Acc</td>
<td>8577</td>
</tr>
<tr>
<td>% change</td>
<td>-13.1</td>
<td>-3.1</td>
</tr>
<tr>
<td>Knapsack</td>
<td>Con. Acc</td>
<td>7672</td>
</tr>
<tr>
<td></td>
<td>Dataflow Acc</td>
<td>8089</td>
</tr>
<tr>
<td>% change</td>
<td>+5.4</td>
<td>+17.3</td>
</tr>
<tr>
<td>Floyd-Warshall</td>
<td>Con. Acc</td>
<td>2491</td>
</tr>
<tr>
<td></td>
<td>Dataflow Acc</td>
<td>7659</td>
</tr>
<tr>
<td>% change</td>
<td>+207.5</td>
<td>+104.3</td>
</tr>
<tr>
<td>DFS</td>
<td>Con. Acc</td>
<td>4810</td>
</tr>
<tr>
<td></td>
<td>Dataflow Acc</td>
<td>8509</td>
</tr>
<tr>
<td>% change</td>
<td>+76.9</td>
<td>+58.5</td>
</tr>
</tbody>
</table>

The difference in area between the dataflow accelerators and the conventional accelerators is effected by two factors. When the dataflow architectural template is used, there are always additional costs associated with the communication channels. Meanwhile, as the original programs are partitioned into subgraphs and separately turned into hardware, the depth of the internal pipeline in each module is reduced, resulting in area savings. The overall change therefore depends on which factor plays a larger role, and is ultimately application specific.

6. CONCLUSION

This paper presents a new architectural template that can be used as an intermediate target for high level synthesis. The accelerators generated using our method run significantly faster than conventional accelerators as computation and communication are automatically overlapped. Overall, our new approach produces hardware engines with an average 5.6 times performance advantage over normal HLS with no intermediate architecture mapping.

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7. REFERENCES